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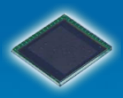
PCC030K 0.3MP Product Brief



The PCC030K is single chip of CIS and ISP. It is a low-cost, high-performance analog and digital image sensor designed specifically for rear view camera applications.

The PCC030K is a 1/6.62-inch CMOS image sensor with NTSC/PAL transmitter. It is a single chip with an effective pixel array of 644 (width) x 484 (height) in an ultra-compact module size, making it an ideal camera solution for rear-view systems.
The PCC030K can generate a digital/composite data at maximum frame rate of 60 FPS. On-chip sensor functions can be controlled through I2C interface.

The output interface of PCC030K is DVP 8-bit, CVBS
It supports auto black level compensation, horizontal/vertical mirroring, automatic flicker cancellation.

Applications

- Rear view camera

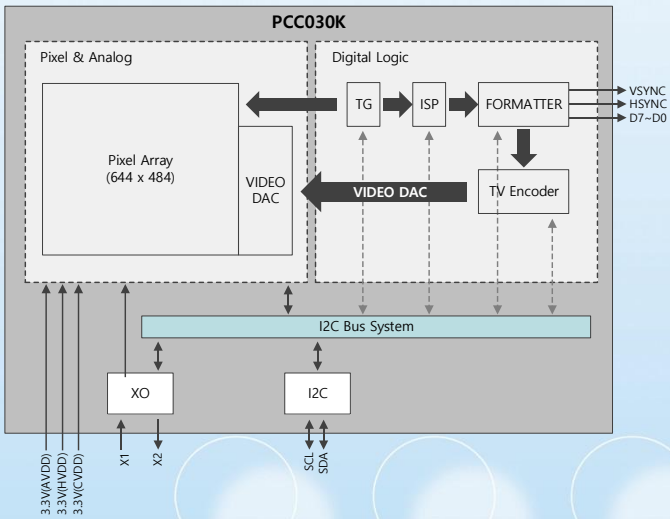
Product Features

- 644x484 effective pixel array with RGB bayer color filters and micro-lens
- Output Interface : DVP 8-bit, CVBS
- Auto black level compensation support
- Horizontal/vertical mirroring support
- Image processing on chip : lens shading compensation, gamma correction, defect correction, color correction, NR(2D noise reduction), color interpolation, edge enhancement, brightness, contrast, de-color, auto white balance, auto exposure control, back light compensation, color saturation
- Automatic flicker cancellation support
- On-chip phase locked loop(PLL)
- I2C interface(master/slave) support
- Crystal input support

Technical Specifications

Parameter	Typical value
Pixel size	3.4 um x 3.4 um
Effective pixel array	644(H) x 484(V)
Effective image area	2.189 mm x 1.645 mm
Optical format	1/6.62 inch
Input clock frequency	27 MHz
Output interface	DVP 8-bit Raw RGB Bayer 8-bit YCbCr422 8-bit Y only 8-bit
	CVBS NTSC PAL
Max. frame rate	60 fps
Dark signal	54 sec@60[°C]
Sensitivity	34K [e/lux*sec]
Power supply	AVDD 3.3V, IO 3.3V, CVDD 3.3V
Power consumption	200 [mW] @ dynamic(CVBS) 125 [mW] @ dynamic(DVP) 660 [uW] @ standby
Operating temp. (Fully functional temp.)	- 40 [°C] ~ 85 [°C] (Ambient)
Dynamic range	64 [dB]
SNR	45 [dB]
Package type	CSP 20ball

Functional Block Diagram



Crystal Image through Imaging **Innovation**

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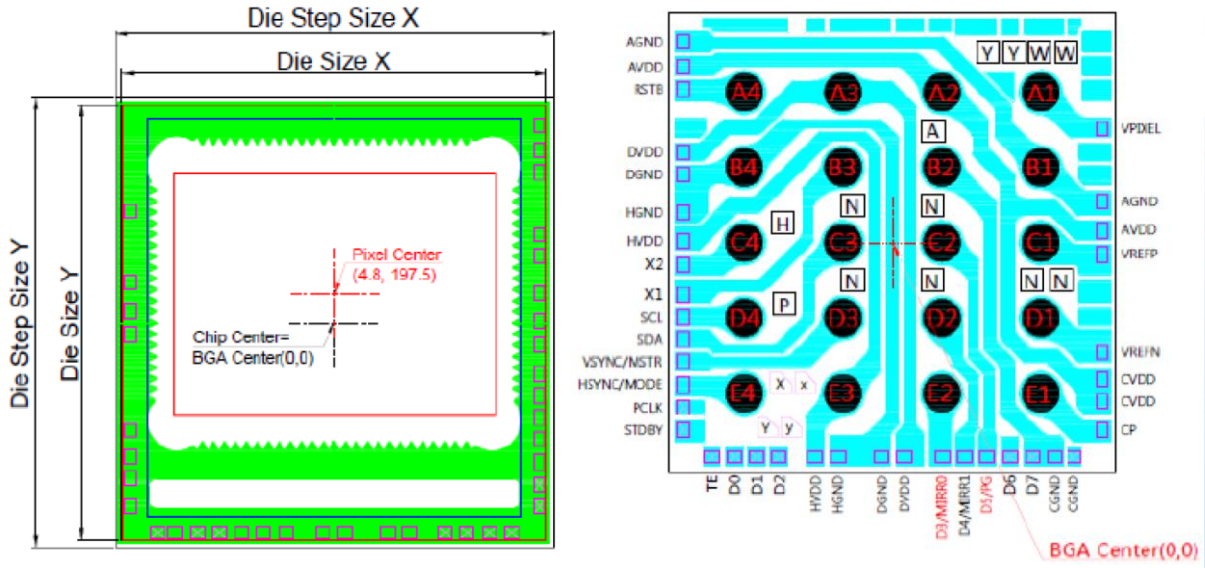
Pad and ball formation

- Package size : 2937 um x 3008 um 20 ball



Package ball assignment table

Ball	Ball name	I/O type	Pull up/ pull down	PAD description
A1	VPIXEL	O	-	PIXEL VDD. It should be tied with nearby AGND by both 1uF bypass capacitors.
A2	AVDD	P	-	Analog VDD 3.3V
A3	DVDD	P	-	Digital(core) VDD 1.2V DC (internal LDO output)
A4	RSTB	I	Pullup	System reset must remain low for at least 8 master clocks after power is stabilized. When the sensor is reset, all registers are set to their default values.
B1	AGND	P	-	Analog GND
B2	CGND	P	-	VDAC GND
B3	X1	I	-	Crystal input pad or master clock input pad
B4	HGND/ DGND	P	-	IO GND / digital(core) GND
C1	VREFP	O	-	PCP output. It should be tied with nearby RGND by both 1uF bypass capacitors.
C2	D5/PG	BIO	Pulldown	Digital output bit 5 / strap input pad : PG mode
C3	SDA	BIO	Pullup	2-wire serial interface data, SDA line is pulled up to HVDD by off-chip resistor.
C4	X2	O	-	Crystal output pad
D1	VREFN	O	-	NCP output. It should be tied with nearby RGND by both 1uF bypass capacitors.
D2	D4/MIRR1	BIO	Pullup	Digital output bit 4/ strap input pad : mirror mode[1]
D3	VSYNC/ MSTR	BIO	Pullup	Vertical synchronization pulse. VSYNC indicates the start of a new frame / MSTR is the strap input pad for master mode.
D4	SCL	BIO	Pullup	2-wire serial interface clock, SCL line is pulled up to HVDD by off-chip resistor.
E1	CP	O	-	Composite differential positive signal Make the total resistance value to 37.5ohm(or 75ohm according to register setting)
E2	D3/MIRR0	BIO	Pulldown	Digital output bit 3 / strap input pad : mirror mode[0]
E3	HVDD	P	-	IO VDD 3.3V DC
E4	HSYNC/ MODE	BIO	Pullup	Horizontal synchronization pulse. HSYNC is high(or low) for the horizontal window of interest. It can be programmed to appear or not outside the vertical window of interest. / MODE is the strap input pad for frame mode.