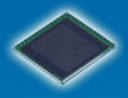
PIXELPLUS

PX9210K 2.0MP Product Brief



The PX9210K is single chip of CIS and ISP. The PX9210K has excellent noise performance for low light condition and high dynamic range support by 2-exp line based HDR mode up to 120dB

The PX9210K is the 1/2.92" RGB bayer CMOS image sensor (CIS) designed to support 2.0MP at 30 frames per second (fps).
The PX9210K consists of 1960 (H) x 1120 (V) effective pixels with 12 added active pixels on each side and 8 pixels on each side for color interpolation.
The PX9210K has excellent noise performance for low light condition and high dynamic range (HDR) support using by DCG (Dual Conversion Gain) and multi- exposure method up to 120dB.
The PX9210K is suitable for a rear view camera and surround-view camera, home appliances and security applications with excellent image quality with 3.3V/2.8V/1.2V power supply.

It incorporates on-chip CIS functions such as Defective Pixel Correction (DPC), Purple Fringing Reduction (PFR), exposure control, HDR combine reconstruction, and so on. It enables the PX9210K shows no saturation image in the worst contrast situations.
It enhances HDR images with local tone map and provides excellent low light image with advanced noise reduction filter. It supports output interface and HD analog video with embedded video DAC

Applications

- Rear View Camera
- 360° Surround View Monitoring System (SVM)
- Security
- Home appliances

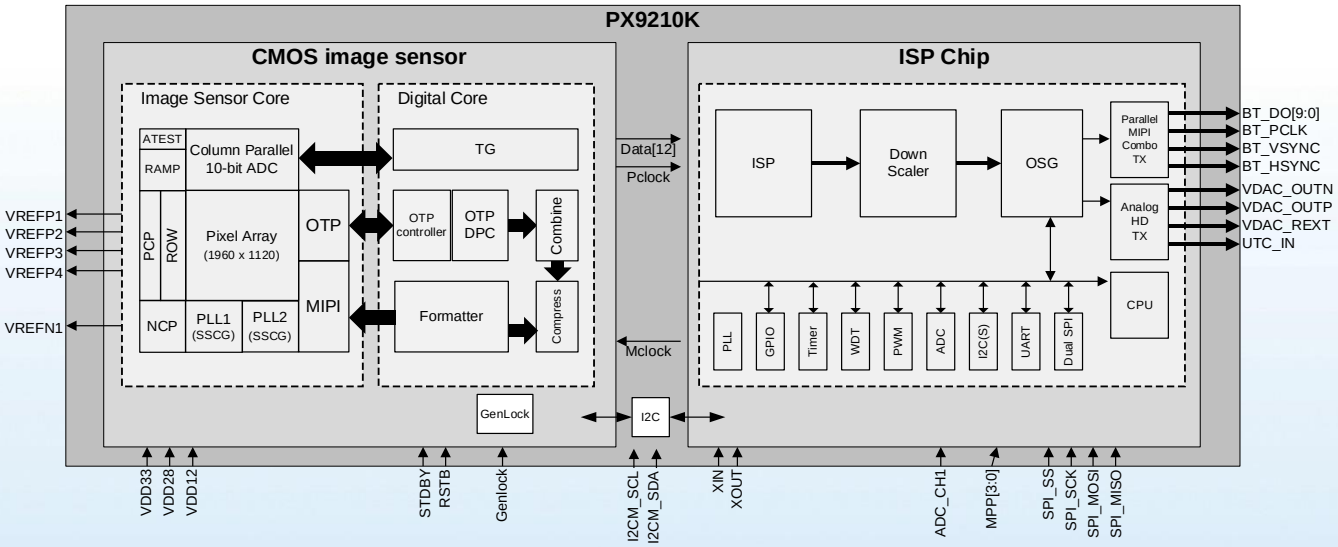
Product Features

- Support for display image size 1920 x 1080 with 2.0MP
- Support for HDR 120 dB with DCG and multi exposure.
- Support for combined RGB bayer output format
- ISP function : LSC, DPC, PFR, HDR combination, automatic black level correction, compression, etc
- Programmable frame size, window size, and exposure
- External synchronization support (Genlock)
- One-time programmable memory (OTP)
- Active Dummy Array for offset correction
- Spread Spectrum Clock Generation (SSCG)

- Image Signal Processing
  - ✓ HDR Tone-map
  - ✓ BLC, LSC, DPC
  - ✓ 2D Noise Reduction
  - ✓ De-mosaic
  - ✓ Color / Gamma Correction
  - ✓ De-color, Edge Enhancement
  - ✓ Contrast & Brightness Control
  - ✓ Hue & Saturation Control
  - ✓ BW Mode
  - ✓ Auto Flicker detection
  - ✓ AE/AWB Static Engine

- CIS Input
  - ✓ MIPI or Parallel Input
    - Up to 1920x1080p@60Hz
    - MIPI CSI-2 RAW 10/12/14/16/20 Bits
    - MIPI CSI-2 1/2/4 Lane @ 600Mbps
    - Parallel 10/12 Bits with H/V Sync
- Video Output
  - ✓ High Quality Free Down Scaling Engine
    - 1080p/960p to 960p/720p
    - 1080p/960p/720p to SD (NTSC/PAL)
  - ✓ MIPI or Parallel Output
    - Selectable between scaler in and scaler out
    - Up to 1920x1080p@60Hz
    - MIPI CSI-2 RAW 10/12 Bits, YUV 16 Bits
    - MIPI CSI-2 1/2/4 Lane @ 450Mbps
    - Parallel 10/12/16 Bits with H/V/F Sync
  - ✓ Analog HD Output
    - Selectable between scaler in and scaler out
    - Up to 1920x1080p @30fps
    - Video DAC with 10 Bits
    - Bi-directional UTC
- Graphic Overlay
  - ✓ 1-BMP (RLE) Layer
    - 4 Area (none-overlap)
    - Parking Guide Line
  - ✓ 1 Font Layer
    - Font Width 16, 24 supported
  - ✓ Private Zone Mask
    - Programmable 8-zones
    - Minimum 8x8 pixels
- External Interface
  - ✓ UART 1 Ch
  - ✓ Timer 4 Ch
  - ✓ WDT 1 Ch
  - ✓ Single / Dual SPI
  - ✓ I2C Serial Interface
  - ✓ Interrupt Controller
  - ✓ GPIOs
  - ✓ DMA

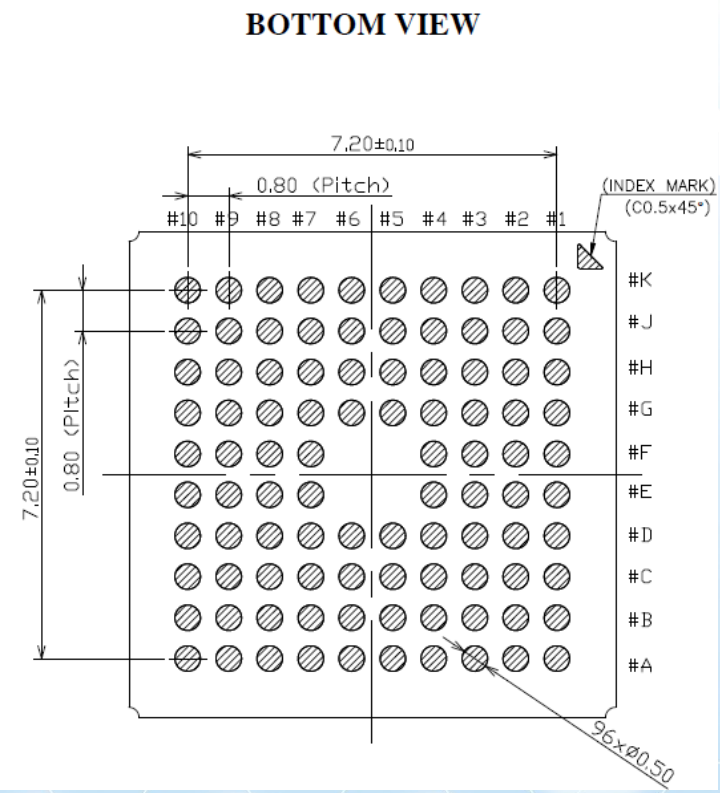
Functional Block Diagram



Technical Specifications

Parameter	Typical value
Pixel size	2.8 um x 2.8 um
Effective pixel array	1960(H) x 1120(V)
Effective image area	5.4880 mm x 3.1360 mm
Optical format	1/2.92 inch
CRA	23.7 °
Input clock frequency	27 MHz
Output interface	2-Lane MIPI / DVP Combo
Max. frame rate	HDR 30 fps only
Dark Current	23 e-/sec @60℃
Sensitivity	30.3K e-/Lux. sec
Power supply	HVDD : 3.3V
	AVDD : 2.8 V
	DVDD : 1.2 V
Power consumption @30fps (HVDD = 1.8V / HVDD = 2.8V)	DPV : 204mW / 234mW MIPI : 201mW / 202mW Standby : 2mW /2mW
Operating temp.	-40 ~ 105 °C (Ambient)
Max. dynamic range	120 dB
SNR	44 dB @60℃
Package type	AmCBGA
Package size	9.5 x 9.5 mm

AmCBGA Ball Map



AmCBGA Ball Assignment Table

Ball	Ball Name	IO	Ball Description
A1	NC		
A2	OVDD	P	Analog VDD 2.8V for OTP It should be tied with nearby OGND by 1uF bypass capacitors.
A3	OGND	P	Analog GND for OTP
A4	STDBY	I	Power stdby mode. When Stdby ='1', there's no current flow in any analog circuit branch, neither any beat of digital clock.
A5	DVDD	P	Digital (Core) VDD 1.2V DC It should be tied with nearby VSS by 1uF bypass capacitors.
A6	VDDO3	P	3.3V BT I/O Power
A7	DVDD	P	Digital (Core) VDD 1.2V DC It should be tied with nearby VSS by 1uF bypass capacitors.
A8	VSS	P	IO GND/Digital(Core) GND
A9	VDDO	P	IO VDD 3.3V DC It should be tied with nearby VSS by 1uF bypass capacitors.
A10	NC		
B1	VSS	P	IO GND/Digital(Core) GND
B2	VREFP3	O	VREFP3 output. It should be tied with nearby AGND by 1uF bypass capacitors.
B3	VREFP4	O	VREFP4 output. It should be tied with nearby AGND by 1uF bypass capacitors.
B4	BT_DO_9	BIO	BT_DO[9] or MIPI_TX_CKN Output
B5	BT_DO_7	BIO	BT_DO[7] or MIPI_TX_DN0 Output
B6	BT_DO_5	BIO	BT_DO[5] or MIPI_TX_DN1 Output
B7	VSS	P	IO GND/Digital(Core) GND
B8	BT_DO_3	BIO	BT_DO[3] or MIPI_TX_DN2 Output
B9	BT_DO_1	BIO	BT_DO[1] or MIPI_TX_DN3 Output
B10	DVDD	P	Digital (Core) VDD 1.2V DC It should be tied with nearby VSS by 1uF bypass capacitors.
C1	NC		
C2	VREFP1	O	VREFP1 output. It should be tied with nearby AGND by 1uF bypass capacitors.
C3	VREFP2	O	VREFP2 output. It should be tied with nearby AGND by 1uF bypass capacitors.
C4	BT_DO_8	BIO	BT_DO[8] or MIPI_TX_CKP Output
C5	BT_DO_6	BIO	BT_DO[6] or MIPI_TX_DP0 Output
C6	BT_DO_4	BIO	BT_DO[4] or MIPI_TX_DP1 Output
C7	VDDI	P	1.2V Core Power
C8	BT_DO_2	BIO	BT_DO[2] or MIPI_TX_DP2 Output

Ball	Ball Name	IO	Ball Description
C9	BT_DO_0	BIO	BT_DO[0] or MIPI_TX_DP3 Output
C10	I2CM_SDA	BIO	Sensor I2C Master SDA
D1	NC		
D2	VREFN1	O	VREFN1 output. It should be tied with nearby AGND by 1uF bypass capacitors.
D3	VDDI	P	1.2V Core Power
D4	VSS	P	IO GND/Digital(Core) GND
D5	VSS	P	IO GND/Digital(Core) GND
D6	VSS	P	IO GND/Digital(Core) GND
D7	VSS	P	IO GND/Digital(Core) GND
D8	VSS	P	IO GND/Digital(Core) GND
D9	VDDI	P	1.2V Core Power
D10	I2CM_SCL	BIO	Sensor I2C Master SCL
E1	DVDD	P	Digital (Core) VDD 1.2V DC It should be tied with nearby VSS by 1uF bypass capacitors.
E2	VDDO3	P	3.3V BT I/O Power
E3	BT_PCLK	BIO	BT PCLK Output
E4	VSS	P	IO GND/Digital(Core) GND
E5	-		
E6	-		
E7	VSS	P	IO GND/Digital(Core) GND
E8	VDDO	P	IO VDD 3.3V DC It should be tied with nearby VSS by 1uF bypass capacitors.
E9	REXT	O	External Resistor for MIPI
E10	VDDO	P	IO VDD 3.3V DC It should be tied with nearby VSS by 1uF bypass capacitors.
F1	AGND	P	Analog GND
F2	BT_VSYNC	BIO	BT VSYNC Output
F3	BT_HSYNC	BIO	BT HSYNC Output
F4	VSS	P	IO GND/Digital(Core) GND
F5	-		
F6	-		
F7	VSS	P	IO GND/Digital(Core) GND
F8	VDDIM	P	1.2V MIPI Rx Core Power
F9	VSS	P	IO GND/Digital(Core) GND
F10	DVDD	P	Digital (Core) VDD 1.2V DC It should be tied with nearby VSS by 1uF bypass capacitors.

Ball	Ball Name	IO	Ball Description
G1	AVDD	P	Analog VDD 2.8V It should be tied with nearby AGND by both 1uF bypass capacitors.
G2	SPI_SS	BIO	SPI Slave Select
G3	SPI_SCK	BIO	SPI Slave Clock
G4	VSS	P	IO GND/Digital(Core) GND
G5	VSS	P	IO GND/Digital(Core) GND
G6	VSS	P	IO GND/Digital(Core) GND
G7	VSS	P	IO GND/Digital(Core) GND
G8	UTC_IN	I	UTC Video Input
G9	VDAC_OUTN	O	Video DAC Negative Output
G10	DVDD_PLL	P	PLL VDD 1.2V DC It should be tied with nearby VSS by 1uF bypass capacitors.
H1	AGND	P	Analog GND
H2	SPI_MOSI	BIO	SPI Master Output Slave Input
H3	SPI_MISO	BIO	SPI Master Input Slave Output
H4	VSS	P	IO GND/Digital(Core) GND
H5	MPP[3]	BIO	UART TX
H6	XOUT	O	Crystal Output
H7	VDDI	P	1.2V Core Power
H8	ADC_CH1	I	GADC CH1 Input
H9	VDAC_OUTP	O	Video DAC Positive Output
H10	AVDD	P	Analog VDD 2.8V It should be tied with nearby AGND by both 1uF bypass capacitors.
J1	VSS	P	IO GND/Digital(Core) GND
J2	TEST	I	Test Enable
J3	RSTB	I	System reset must remain low for at least 8 master clocks after power is stabilized. When the sensor is reset, all r egisters are set to their default values.
J4	MPP[1]	BIO	I2CS_SDA
J5	MPP[2]	BIO	UART RX
J6	XIN	I	Crystal Input
J7	VDD3P	P	PLL 3.3V Power
J8	VDD3V	P	Video DAC 3.3V Power
J9	VDAC_REXT	I	Video DAC Rext Load
J10	AGND	P	Analog GND
K1	NC		
K2	DVDD	P	Digital (Core) VDD 1.2V DC It should be tied with nearby VSS by 1uF bypass capacitors.

Ball	Ball Name	IO	Ball Description
K3	DVDD	P	Digital (Core) VDD 1.2V DC It should be tied with nearby VSS by 1uF bypass capacitors.
K4	MPP[0]	BIO	I2CS_SCL
K5	VDDO	P	IO VDD 3.3V DC It should be tied with nearby VSS by 1uF bypass capacitors.
K6	VDDO1	P	3.3V Digital I/O Power
K7	GENLOCK	BIO	External Frame sync input. Slave chip can receive the external frame sync signal from master chip/External Frame sync output. Master chip can output the external frame sync signal through this pad to synchronize all digital outputs of two or more chips
K8	DVDD	P	Digital(Core) VDD 1.2V DC It should be tied with nearby VSS by 1uF bypass capacitors.
K9	VSS	P	IO GND/Digital(Core) GND
K10	NC		